Circuit arrangement for driving a display arrangement

The invention concerns a circuit arrangement for driving a display arrangement. Further it concerns a display arrangement and a method for driving a display arrangement.

The display technique will play an increasingly important role in the information and communication technique in the years to come. Being an interface between humans and the digital world, the display device is of crucial importance for the acceptance of contemporary information systems. Notably portable apparatus such as, for example, notebooks, telephones, digital cameras and personal digital assistants cannot be realized without utilizing displays.

In general a liquid crystal display consists of a number of substrates. The display is subdivided in the form of a matrix of rows and columns. The row electrodes and column electrodes are arranged on respective substrates and form a grid. A layer with liquid crystals is provided between said substrates. The intersections of these electrodes form pixels. These electrodes are supplied with voltages that orient the liquid crystal molecules of the driven pixels in an appropriate direction so that the driven pixel appears in a different brightness.

There are two kinds of LC display arrangements- the passive matrix displays and the active matrix displays. The passive matrix LCD technology is a very commonly used display technology; it is used, for example in PDA's and in mobile telephones. Passive matrix displays are usually based on the (S)TN (Super Twisted Nematic) effect.

The active matrix displays also called TFT displays using a switching element within each pixel, which is commonly realized as a thin film transistor.

There are other kinds of display technologies, e.g. OLED, PLED or LTPS also having rows and columns arranged in matrix form.

In all kinds of display arrangements the image data to be displayed will be provided via the column electrodes. These column electrodes are driven by a column

driver, which converts the image data supplied from a memory or an external device into the respective column voltage, which are necessary to drive the certain pixels of a selected row. The column driver means comprises a converting unit e.g. a digital analog converter, which converts the image data provided from the memory into analog signals. The column electrodes are driven by output channels. An output channel includes in particularly an amplifier or output buffer for amplifying the analog low level image signal to the respective column voltage level. Further a selection matrix is arranged for providing all possible column voltages to the output channel, wherein the respective column voltage is chosen via the selecting matrix.

For displaying a clear, high quality image it is very important to drive the column electrodes with well calibrated output channels without any offsets. Therefore each column output channel of the column driving means has to be calibrated before settling the required column voltage in dependency on the pixel value or image data to be displayed. The output channels normally having a mismatch between an input stage of the output buffers or a mismatch between the resistive elements in the DA-Converter. Further the offsets will be affected by process variations during manufacturing of the driver circuit.

A further problem for the calibration of the column output channels is that the time available for the calibration should be as short as possible, because the time is needed for settling respective column voltage output signal. Besides this the sampling of the column voltage is performed few microseconds before the load pulse (LD) to improve the cleanness of the column output signal, because of the data changing. Considering this situation leaves only 4-6μs for offset cancellation. If this offset cancellation is not performed properly a degradation of the illustrated image is the result, because a difference of more then 7mV in the column voltage is visible.

So the object ~~of the present invention~~ is to provide an arrangement having a good offset cancellation combined with high quality illustrating of an image. In particularly the time required for settling the column voltage should be as long as possible, without being reduced by the time required for offset cancellation.

To solve this object a circuit arrangement is provided for driving a display arrangement, the circuit arrangement includes column driving means for driving n column electrodes and row driving means for driving m row electrodes, wherein the column driving means comprises n output channels, each output channel having a column electrode assigned and is arranged for providing a respective column voltage to the assigned column electrode. Further an additional output channel is arranged for providing a respective column voltage, whereas each of the n column electrodes is connectable to the additional output channel.

The invention is based on the idea, that the time for offset cancellation for each output channel before loading the respective column voltage is too short and an offset cancellation within that short time will degrade the image quality. Therefore the additional output channel will be provided within the column driving means. This allows calibrating at first the additional output channel, whereby all other output channels could then be successively replaced by this calibrated additional output channel, whereas at the time the output channel is replaced by the additional output channel the normal output channel will be calibrated. Thus all output channels will be calibrated sequentially, without reducing the time for settling the column voltage. The time for calibrating is long enough, because the switching between the output channels and the additional output channel will be performed with the row selecting procedure of the row electrodes.

During the first row selection time the additional channel is calibrated. Then the column 1 is connected with the calibrated additional channel. Then the next row is driven, whereas during that time the disconnected first column output channel is calibrated. So the first column is driven with a calibrated additional channel. Before driving the third row the additional channel is connected to the next column output channel (column 2) and the first column output channel is connected to the first column electrode again, because it is calibrated now. During driving the third row the second column electrode will be driven via the calibrated additional channel, whereas the first column is driven by its own calibrated first column output channel, whereas the second column output channel is just calibrated. This procedure will go on, until all column output channels are calibrated. Thus the time for calibrating an output channel is much

longer than before. In particularly the time for offset cancellation is as long as a row is driven.

Since normally a display arrangement will have more columns than rows, more than one frame will be required until all output channels will be calibrated. The frame rate can be in the range of 60-85Hz. However in view of the advantages this is an acceptable time. When the number of rows is greater or equal than the number of output channels divided by the number of additional output channels the calibration procedure will be completed within one frame.

The use of the additional output channel does not require more output channels to be designed, because the additional output channel is a not actively used output channel of the column driver, which is arranged within each column driving means, so called dummy output channels, which are used normally to maintain the matching between the output channels.

In a preferred embodiment of the invention switching means are arranged between an output channel and its associated column electrode for connecting the column electrode with the additional output channel. These switching means are provided for disconnecting the output channels from the column electrodes, if the column electrode is connected to the additional output channel. The controlling of the switches is done by a logic circuitry, which does not need much chip area and could be implemented into the normal logic circuitry within the driving means.

In a further preferred embodiment of the invention the additional output channel is calibrated at the beginning of driving a first row electrode of a frame, whereas during driving the following row electrodes the additional output channel is successively connected via the respective switching means to the remaining not calibrated column electrodes, whereas the associated output channel of the column electrode currently connected to the additional output channel is disconnected from the respective column electrode for calibrating.

In a further preferred embodiment of the invention the column driving means comprises more then one additional output channel which are connectable to the column electrodes. This will reduce the time for calibrating all output channels, because during one row selection time two output channels could be calibrated.

For calibrating the additional output channel and the output channels calibration means are arranged in particular for performing the offset cancellation of the output channels connected to the calibration means.

The object is also solved by a display device comprising a display arrangement and a display driver circuit arrangement, the display driver circuit arrangement comprises column driving means for driving the n column electrodes with column voltages and row driving means for driving the m row electrodes with row selection voltages, wherein the column driving means comprises n output channels, each output channel having a column electrode assigned and is arranged for providing a respective column voltage to the assigned column electrode, an additional output channel is arranged for providing column voltages, whereas each of the n column electrodes is connectable to the additional output channel.

The object is further solved by a method for driving a display arrangement, whereas the display arrangement comprises n column electrodes and m row electrodes, the n column electrodes are driven by column driving means and the row electrodes are driven by row driving means, wherein the column driving means comprises n output channels each providing a respective column voltage to its associated column electrode, wherein an additional output channel is arranged which is calibrated at the beginning of a driving procedure of a frame, wherein after the additional output channel is calibrated, one of the n output channels is disconnected from its associated column electrode, wherein this column electrode is connected to the calibrated additional output channel, the calibrated additional output channel supplies the respective column voltage to the column electrode, whereas the disconnected output channel is calibrated.

Depending on the used calibration scheme the inventive calibration procedure has to be done several times.

The inventive circuit arrangement is also applicable for other display solutions like OLED (Organic Light Emitting Diode) or PLED (Polymer Light Emitting Diode) or LTPS (Low Temperature Poly Silicon).

For a more complete description of the present invention and for further objects and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, in which:

Fig. 1 shows a schematic diagram of a display device;
Fig. 2 shows output channels of the column driver according to the present invention;
Fig. 3 shows an alternative embodiment of a column driver according to the present invention;
Fig. 4 shows a timing diagram for calibration;

Figure 1 shows an electric circuit diagram of a display device comprising a display arrangement 1 and a display driver circuit arrangement 2. The display arrangement 1 comprises a matrix of pixels 8 defined by the areas of crossings of row or selection electrodes R and column or data electrodes C. The display driver circuit arrangement 2 includes a row driver 4, which supplies row selection voltages or mutually orthogonal functions to the m row electrodes Rm. Further a column driver 5 is arranged within the display driver circuit arrangement 2. The column driver 5 supplies column voltage levels according to data to be displayed to the n column electrodes C. To this end, incoming data are first processed, if necessary, in a processor or logic circuitry 3. Mutual synchronization between the row driver 4 and the column driver 5 takes place via control lines 9. The calibration means 10 for performing the calibration in particularly the offset cancellation are arranged within the logic circuitry 3.

Figure 2 shows a first embodiment of a column driver 5 according to the present invention. The column electrodes are designated with C_1- C_n. The column driver 5 includes n output channels O_1- O_n, whereas each output channel O_1- On is associated to its column electrode C_1- C_n. Further a DAC is illustrated, which converts the digital data into analog data. Between each column electrode C and the associated output channel O a switch S is arranged. The switches S_1-S_n are capable to disconnect the output channels O_1-O_n from their column electrodes C_1- C_n. The additional output channel O_R is arranged, whereas the additional output channel O_R is also capable to provide a respective column voltage to a column electrode to which it is connected.

The image data will be supplied via the control line 9 to the DA-Converter DAC. The image data for the respective column C, in particular for the pixel in the selected row, which is currently selected, will be provided to the output channel O of this column C. The output channel O comprises a selection matrix for choosing the respective required column voltage, which is supplied to the incorporated output buffer or amplifier, which are not illustrated. The amplified analog signal, which represents the respective column voltage for the pixel is supplied via the switch S to the column electrode C. The additional output channel O_R can be switched to each of the column electrodes C_1-C_n.

In the case that the additional output channel O_R is connected to one of the column electrodes C, e.g.C_2, the image data to be displayed at the selected pixel of this column electrode C_2 is feed to the additional output channel O_R. Further the respective output channel O_2 of the column electrode C_2 will be disconnected from this column electrode. During a row selection time the output channel O_2 will be connected to calibration means 10 for offset cancellation. During the next row selection time the calibrated output channel O_2 is connected to its associated column electrode C_2 to drive this column with the required column voltage in dependency of the image data to be displayed. Simultaneously at this row selection time a further column output channel O, e.g. O_3, will be disconnected from its column electrode C_3 for being connected with the calibration means 10 for calibrating. This column electrode C_3 is driven instead by the additional output channel O_R. So after n row selection times all output channels O will be calibrated.

To avoid this probably long time it could be advantageous to use more than one additional output channel O_R. Such embodiment is shown in Figure 3. In general the shown column driver 5 comprises the same components as the column driver shown in figure 2. Due to the simplicity only six column electrodes C_1- C_6 are shown, having their switches S_1- S_6 and their output channel channels O_1- O_6. In this embodiment two additional output channels O_{RL} and O_{RR} are included. That means during selection of the first row both additional output channels O_{RL} and O_{RR} will be calibrated. During the second row selection time C_1 and C_6 are driven by the additional output channels O_{RL} and O_{RR} respectively. The output channels O_1 and O_6 are disconnected from their column electrodes for being connected to the calibration means

10. At next the column electrodes C_2 and C_5 are driven by the additional output channels O_{RL} and O_{RR}, whereas the associated output channels O_2 and O_5 will be calibrated. So after four row selection times all 6 column output channels are calibrated.

Figure 4 shows a calibration timing diagram for the calibration procedure. LD designates the load pulse for loading the data into the column driver so the equivalent column voltages derived from the DAC are applied to the output channels of the driver, which are valid for an entire row selection time. The time between two load pulses LD is the row selection time. Directly after the first load pulse LD the additional output channels O_{RL} and O_{RR} will be calibrated. The calibration stops with the next load pulse LD. At next the output channels O_1 and O_6 are calibrated, then the output channels O_2 and O_5 and output channels O_3 and O_4. After the calibration of all output channels O1- O_6 the procedure starts again with the calibration of the output channels O_{RR} and O_{RL}.